IN THE CLAIMS

Claims 21 and 29-40 are pending. Claims 21, 29, 35, 37, and 38 have been amended. A complete list of claims with amendments marked up is presented below:

Current Listing of Claims

Claims 1-20. (Canceled)

21. (Currently amended) A system, comprising:

a bus;

a processor including a plurality of machine specific registers, wherein each one of the plurality of machine specific registers is associated with one or more functional units of the processor, said processor to execute an instruction that updates ~~microcode~~ at least one microinstruction by changing a value of at least one bit in at least one of said plurality of machine specific registers ; and

a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store said instruction.

Claims 22-28. (Canceled)

29. (Currently amended) A method, comprising:

storing an instruction that, when executed on a processor, updates ~~microcode~~at least one microinstruction, on a computer readable medium external to said processor;

executing said instruction to update the ~~microcode~~ at least one microinstruction using the processor, wherein the processor includes a plurality of machine specific registers associated with at least two functional units of the processor; and

controlling one of the at least two functional units of the processor in response to executing said instruction to update the ~~microcode~~ at least one microinstruction by modifying a value of at least one bit included in one of the plurality of machine specific registers.

30. (Previously presented) The method of claim 29, wherein modifying a value of at least one bit included in one of the plurality of machine specific registers associated with one of the at least two functional units of the processor operates to affect the behavior of an other one of the at least two functional units of the processor.

31. (Previously Presented) The method of claim 29, wherein a logical source register and a logical destination register for executing said instruction are selected from the plurality of machine specific registers.

32. (Previously Presented) The method of claim 29, wherein the at least two functional units are linked by a communication bus to a data control unit to fetch said instruction from the computer readable medium.

33. (Previously Presented) The method of claim 29, wherein controlling one of the at least two functional units of the processor in response to executing the instruction further includes:

controlling a non-performance critical function.

34. (Previously presented) The method of claim 33, wherein the non-performance critical function is selected from the group consisting of:

cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions.

35. (Currently amended) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

storing an instruction that, when executed by a processor, updates ~~microcode~~at least one microinstruction, in memory external to said processor;

executing said instruction to update the ~~microcode~~ at least one microinstruction by the processor;

updating one or more machine specific registers associated with a logic unit on the processor in response to the executing of said instruction; and

controlling one or more functions of the logic unit on the processor based on a value stored in the one or more machine specific registers.

36. (Previously presented) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

moving a value from a general purpose register of the processor to the one or more machine specific registers.

37. (Currently amended) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

~~reprogramming the microcode in~~fetching the at least one microinstruction from firmware of said processor.

38. (Currently amended) A processor, comprising:

a first logic unit; and

at least two machine specific registers associated with the logic unit, the at least two machine specific registers to trigger processor hardware logic functions when a selected one of the at least two machine specific registers is updated in response to executing an instruction that, when executed by said processor, updates ~~microcode~~ at least one microinstruction of said processor fetched from a memory external to the processor.

39. (Previously Presented) The processor of claim 38, further comprising:

a second logic unit associated with a selected one of the at least two machine specific registers.

40. (Previously Presented) The processor of claim 39, wherein changing a value of at least one bit in a selected other one of the at least two machine specific registers affects the behavior of the second logic unit.